

ABSTRACT

A plurality of sensor chips, each having strain gauges and a thin diaphragm, are formed on a semiconductor wafer having an upper layer and a lower layer forming a P-N junction plane therebetween. The sensor chips are separated into individual pieces by dicing along column and row interstices dividing the sensor chips. Conductor lines for supplying an electrical voltage for electrochemically etching the diaphragms are formed on and along the interstices. All of the conductor lines are removed by a dicing blade having a wider width than the conductor lines to avoid electrical leakage due to particles of conductor lines leftover on side surfaces of the diced out sensor chips.